REMARKS

Present Status of Application

Claims 1-16 remain pending in the application. The Office Action mailed on September 27, 2005 rejected claims 1-16 and objected claim 12. Claim 12 is objected because of grammatical error. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Adamic, Jr., U.S. Patent No. 6,124,179 ("Adamic" hereinafter). Claims 2-11 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art. Claims 12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adamic.

Claims 1 and 12 have been amended. Applicant believes that these changes do not introduce new matter and reconsideration of claims 1-16 is respectfully requested. In view of the above amendments and the following discussions, a notice of allowance is respectfully solicited.

Discussion for Claim Objection

Applicant has amended claim 12 and believes now claim 12 is grammatically correct.

Discussion for 35 U.S.C. 103(a) rejections

In regard to claim 1, the description of Figs. 2A-2E of Adamic only mentions "the high resistivity element layer 210" (col. 8, ll. 18-19), and the high resistivity characteristic is only because the layer 210 is a "lightly doped element layer" (col. 11, line 56). When there is need to manufacture different types of transistors, such as NPN and PNP transistors mentioned in Adamic,

a low concentration region has to be formed in another low concentration region. See Adamic, col. 8, ll. 11-12, "A low concentration P-type collector region 232 is formed in element layer 210". And the high resistivity element layer 210 is not designed to be a resistor. Moreover, the resistance in the transistors mentioned in Adamic is designed to be low. See Adamic, col. 3, ll. 44-47, "FIG. 3 is a schematic cross-sectional view of an embodiment of a semiconductor circuit which has a reduced lateral and vertical leadout resistance and is fabricated using the method illustrated in FIGS. 2(a) through 2(f)". Also, cols. 7-8 in Adamic do not mention about forming a CMOS resistor.

On the other hand, the Application is about creating a semiconductor resistor by CMOS process, thus the resistor is denoted as CMOS resistor. And the technology disclosed in the Application is different from that in Adamic. Even the figures of preferred embodiments are different. Adamic discloses two kinds of BJT, whereas the Application discloses a resistor. Adamic is related to inverted dielectric isolation process, whereas the Application is related to fabricating high resistance CMOS resistor.

Thus Applicant believes claim 1 is non-obvious over Adamic and is patentable. Since claims 2-16 are dependent on claim 1 and include all limitations of claim 1, claims 2-16 are also non-obvious over Adamic and are patentable.

In addition to the reasons above, Applicant believes claims 2-11 and 13-15 are patentable for at least the reasons below.

The energy level, concentration of dopant, resistance, temperature, time, molar fraction,

depth, and thickness disclosed in the Application is for achieving the result of a high resistance CMOS resistor, which is a particular, new, and unexpected result in contrast to the prior art. Thus Applicant believes claims 2-11 and 13-15 are patentable.

Reconsideration and withdrawal of these rejections under 35 USC 103(a) are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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